REMARKS

The Examiner is thanked for his extensive and detailed Office Action mailed on June 18, 2003.

The Examiner indicated that the prior response has satisfied the Examiner's requests on all the previous issues which the Examiner had raised and had withdrawn all relevant objections. Applicants greatly thank the Examiner for this indication.

The Examiner also, in making the rejection provided extensive citation to the reference at issue so that a clear understanding between the parties could be reached. Applicants again thank the Examiner for the clear and extensive explanation accompanying the rejection.

New formal drawings have been requested from the client and will be provided shortly.

On page 5, paragraph 12 of the response the Examiner discusses the difference between FLASH memories and EEPROM memories. The Examiner then interprets that the difference between EEPROM and FLASH to be that FLASH can only be erased one block at a time, whereas EEPROM enables smaller element sizes to be erased. Applicants substantially agree with this definition. The term of art used for the smallest block then can be erased in a FLASH memory is the term "sector". Some people may refer to a sector as a block however, in the are and also in the present application, the term used for this grouping of the memory cells is a sector. One of the differences between an EEPROM and FLASH is that a FLASH only permits entire sectors to be erased as groups, whereas an EEPROM permits individual memory cells or other groupings to be erased. Namely, in a FLASH, all memory cells in an entire sector are erased simultaneously and it is not possible to erase less than one entire sector. This definition is seen as substantially the same as the Examiner's.

This definition highlights the differences between the present invention and the prior art. In a NOR or NAND FLASH memory, it is not possible to erase less than one entire sector at a time; this is one of the basic definitions of FLASH. Namely, a sector is defined as that group of memory cells which is the smallest that must be simultaneously erased at the same time. The sector always includes a plurality of blocks of memory cells and each block includes a

plurality of pages. This is to be contrasted with the cited 5,777,923 to Lee et al. (Lee '923 patent).

In the Lee '923 patent, the term "FLASH" as defined herein is not applicable to his modified structure. As Lee points out, known NOR FLASH memories can only perform the erase function simultaneously on many bits at the same time. The Lee et al. '923 patent adds additional structure to his FLASH memory so that it is no longer an actual FLASH memory by the industry standard definition. Figure 2A of the Lee et al. '293 is actually an EEPROM structure. He has basically made an EEPROM structure and still calls it a FLASH. In one embodiment, he uses an "AND plane" with the drain side tunneling both erasing programming. In another embodiment, he adds an additional transistor string which he refers to as an "ELITE ARRAY".

See for example figures 2A and 2B in which he shows that a NOR plane has been constructed as a DINNOR plane in which a further structure has been added, namely an ELITE ARRAY. As the Lee '923 patent points out in column 8, beginning at line 14 his NOR FLASH memory has been modified by adding an additional column of transistors and additional circuit connections and diffusions, which he refers to as "ELITE ARRAY 122". The ELITE ARRAY 122, as shown in figure 9 and also illustrated in figure 2B as an ELITE ARRAY, is an additional array of transistors, which permit further control of the individual memory cells beyond what is possible in a standard NOR FLASH. This ELITE ARRAY is part of the memory array itself and renders the FLASH array outside of NOR FLASH family. In particular, the individual erasability as if it were an EEPROM is not being performed by the NOR FLASH array in Lee et al. '923, but rather is being performed by the ELITE ARRAY, which has been added to a standard NOR FLASH array.

The present invention on the other hand achieves its emulation of an EEPROM memory without the use of an ELITE ARRAY rather, software and a state machine are used to operate a normally FLASH memory sector as if it were an in EEPROM individual bit erasability mode.

Claim 1 has been amended to specify NOR FLASH array and also new claim 24 specifies that NOR FLASH array. These embodiments make clear that these particular claims

apply only to a NOR FLASH array. The NOR FLASH array is a particular structure which is substantially faster in reading than an AND FLASH array. These claims do not apply to a AND FLASH array.

By the Examiner's own definition, an AND FLASH array does not fit the definition of a FLASH array. Since, as Lee points out, his organization of the AND FLASH array permits both the erasing and programming of individual bits, as stated on column 4, line 60-65. The AND FLASH array is substantially slower in many of its operational features, such as programming and most especially reading. Therefore, AND FLASH arrays are not desired in microprocessor and computer applications.

Claim 1 as amended is believed patentable over the prior art of record. In particular, claim 1 distinctly defines over the Lee '923 patent as will now be explained. As specified in claim 1 as originally submitted, the invention is an emulation of an EEPROM memory array. Specifically, a NOR FLASH memory array is used to emulate an EEPROM.

Instead of being an EEPROM, the invention is directed towards emulating an EEPROM using a NOR FLASH memory structure. This distinction departs from the Lee '923 concept. Lee actually modifies his structure by adding an array of memory cells, an ELITE ARRAY 122 (see figure 9 and accompanying description in column 8) or by organizing the FLASH as if it were an EEPROM by putting it into an AND plane. This substantially rewires the connections to the memory cells so that fundamentally, the memory array is no longer in the form of a NOR FLASH array and by its own natural organization can be treated as an EEPROM and addressed for erasure one individual bit at a time. Thus, substantial additional transistor connections are provided in his two structures.

For example, in viewing figure 2A of Lee of the '923 patent the AND structure can be shown to have a bit line connected to each drain of each individual transistor in the array and another bit line connected to each source of each individual transistor in the array thus providing two bit lines per memory cell, and thus two bit lines per column. These are two electrical connections per transistor, one to each of the bit lines per column. This is a large and cumbersome array and is more similar to the organization of an EEPROM rather than a NOR FLASH. Compare the organization of figure 2B to the figure 2A in the Lee et al. '923 patent. In

the organization of figure 2B, a NOR FLASH array there is only one bit line for the entire column of memory cells and in addition, the bit line is only coupled once for every two memory cells so that a single bit line connection is shared between two memory cells. This cuts the number of bit lines in half and thus substantially reducing the size of the memory array. In addition, having only one bit line connection for every two memory cells rather than two for each memory cells reduces the area of the contacts and Vias required by a quarter of the prior amount thus further substantially reducing the area consumed by the NOR array. Thus, the advantage of the NOR array having a very high density with many memory cells per sector is retained in the present invention since the traditional NOR FLASH array structure is maintained.

According to claim 1, the NOR FLASH memory structure has a first selected number of memory cells which are in a first sector. The sector is structured to emulate EEPROM bit alterability, but emulates this bit alterability by using a large number of NOR FLASH memory cells to emulate a single byte of EEPROM memory. Namely, the number of memory cells of the EEPROM, which can be emulated by the FLASH memory is a second selected number, which is much fewer than the number of FLASH memory cells which are required.

Newly submitted claim 21 specifically states that the ratio is 8 to 1. Namely, it requires eight times as many FLASH memory cells to emulate a corresponding number of EEPROM memory cells. Claim 1 as amended thus is distinctly different from Lee '923 because Lee, rather than using a different number of memory cells instead uses one memory cell of the FLASH to act as one cell in EEPROM. He is able to achieve this difference by adding additional structure and electrical connections to the standard NOR FLASH array and thus sacrifices memory array density and consumes more area in the silicon chip. The present invention, on the other hand uses software processing and a state machine in order to perform the emulation at the sacrifice of requiring the use of more NOR FLASH memory cells to emulate a few number of EEPROM memory cells. This concept is entirely missing from Lee '923 patent and, claim 1 is believed to be patentable as presently submitted.

Claim 3 is believed patentable for reasons beyond the patentability of claim 1. In particular, claim 3 specifies that 8 K bits of FLASH memory structure are required to emulate

one K bit of the EEPROM. This particular feature is not suggested by Lee in the '923 patent. The Examiner points to figures 2A and 2B and the associated text as showing this feature. Applicants disagree. Figures 2A and 2B show the addition of an ELITE ARRAY which is not comprised of memory cells. Further, the ELITE ARRAY accomplishes a 1 for 1 correspondence between a memory cell and the individual erasability as if it were an EEPROM. No ratio of 8 to 1 is shown or described in the Lee '923 patent and this claim is believed patentable.

Claim 4 is believed patentable for reasons beyond the patentability of claim 1. Claim 4 specifies that the EEPROM sectors are divided into a first and second EEPROM emulated sectors and that each of these are divided into a pre-determined number of blocks and that each block is divided into a pre-determined number of pages. Sectors can be different sizes, as shown in figure 1 of the present invention. This structure is distinctly different from the structure taught and used in the Lee '923 patent. In particular, Lee's structure of his memory does not include separate blocks and pages, with pages being a subset of blocks. According to Lee, see column 15 and column 16 a block is equated to a page. According to Lee the "page" is the maximum number of bits that can be simultaneously programmed. On the other hand, in the present invention and as defined in claim 4 a page is a subset of a block. In the present invention, the page is the minimum size of bits that can be simultaneously moved from one block to another so as to emulate the bit of erasability. Thus, as defined in claim 4 of the present invention a block is a subset of a sector and a page is a subset of a block, whereas Lee '923 FLASH array is constructed in a very different fashion, which consumes more silicon area for the same number of memory cells.

Claim 5 is clearly patentable over the prior art. Claim 5 specifies a state machine which is provided for controlling an address counter to an internal bus running inside the memory machine macrocell. The Examiner points to column 2, line 45, to column 3, line 7 as teaching the structure of claim 5. Applicants completely disagree. Claim 5 specifically refers to the use of registers, either volatile and non-volatile registers which are read and updated with the addresses under the control of the state machine. Lee has nothing similar. Lee does not provide in his description in columns 2 and 3 or anywhere else in his application the use of a state machine which controls an address counter for an internal address bus and further the address

counter loads the hardcore addresses into registers, which are read and updated by the microcontroller. Nothing in the language that the Examiner has pointed to, nor anywhere else in the Lee '923 patent describes such a state machine, or suggest that one is even possible. Nor, does Lee describe the use of registers for storing the hard-coded addresses under control of an address counter coupled to the memory array. These features are just plain missing from the Lee '923 patent and claim 5 should therefore be allowed.

Claim 6 is patentable for reasons beyond the patentability of claim 5. Lee uses a buffer to store old data so as to avoid the program running the new data if the two data values are equal to each other. See column 6, lines 12-20 as pointed to by the Examiner. Lee's system results in the sensing and storing of old data at different locations and comparing the old data to new data within the memory. Claim 6 is distinctly different and unrelated to this feature. In particular, claim 6 is to a RAM buffer which can communicate with a state machine. This RAM buffer can store not only data, but also stores addresses. Claim 6 specifies that the RAM buffer which is used for page updating also includes "two additional bits for storing a page address during a page updating phase". Nothing in the Lee '923 patent discusses such a RAM buffer which is capable of storing the addresses of the pages in combination with the data being stored. Claim 6 is therefore patentable over Lee '923 patent.

Claim 8 believed clearly patentable in light of the prior art. Claim 8 is a method claim and the sequence of steps start in claim 8 are completely foreign to those which are suggested by the Lee '923 patent. The Examiner points to column 2, lines 45-65 as teaching the feature of "updating the emulating EEPROM memory portion programming different memory locations in a single bit mode". Applicants completely disagrees that such a feature or method step is taught in this portion of the summary of the invention. The place in Lee '923 that the Examiner points to is the summary of the invention which deals with comparing new data to old data. There is certainly no teaching here of swapping the data from one block to another or from one sector to another after one portion has been erased.

Claim 8 goes on to state that "a page update selected page data are moved to a next free block and, when an EEPROM sector is full, all the pages are swapped to another EEPROM sector". The Examiner asserts that such a feature is taught in column 7 of the Lee

'923 patent. Applicants strongly disagree. There is no discussion in the Lee '923 patent regarding the pages being swapped from one EEPROM sector to another. In Lee, the operation is as follows, a selected bit is made and is erased and reprogrammed or alternatively a page or subpage may be erased and reprogrammed. Lee creates a hardware structure to achieve this individual bit addressability. Applicants claim 8 is completely different. Since it is impossible for standard FLASH to individually erase a single bit or byte or even a page, the inventors have proposed the following novel method as specified in claim 8. Namely, the invention proposes to move the bit to the following block and, when the last block is reached the bit is swapped to the other sector and the first sector is erased. This novel feature is claimed in claim 8 and the Lee '923 patent is not similar in any regard.

Claim 10 is believed patentable for reasons beyond the patentability of claim 8 or any other claims in the present application. Claim 10 specifies besides first and second memory portions the additional structure of a plurality of memory pointers each reflecting the memory block, which includes a current memory location and each set of memory locations including a current memory location. Claim 10 further specifies the memory controller structured to, in response to a write request, determining from the memory pointer what is the next memory location following the current memory location from the selected set and then writing data to the next memory location. The Lee '923 has nothing of this type. Lee, in column 7 beginning at line 42 states that a new technique is used to organize the read/write circuit. In particular, he uses a three stage decoder and a predetermined number of read/write circuits are used in order to reduce the writing time. There is no discussion in the Lee '923 patent to a plurality of memory pointers each reflecting which memory block includes a current memory location and the use of the memory controller structured to interactive such memory pointers to select the address assigned to a select one of the memory locations. The Examiner states that the use of page addresses and page pointers is inherent in a process involving storing related pages and subpages. Applicants strongly disagree.

Certainly, Lee '923 patent does not teach such a structure. It is not inherent in the structure either since Lee clearly achieves this function without the use of such pointers. Lee points out in column 2 that he uses a step counter to generate a plurality of step counts and a

word line decoder coupled to the step counter. Far from being inherent, the claimed organization of claim 10 of plurality of memory pointers each respectively reflecting which memory block includes a current memory location and being directed under the control of the memory controller and also being accessible by the memory controller specified in claim 10 is novel and unique. Certainly, the Lee '923 patent achieves his memory array operation without such a memory controller and without such pointers having the claimed specified interaction with the memory controller. Claim 10 is believed patentable in light of the prior art.

Claim 11 is believed patentable on its merits beyond the patentability of claim 10. Claim 11 specifies that there are plurality of pointers for each of the FLASH memory portions and that the FLASH memory portions are a part of the first and second memory sectors. Claim 11 further specifies that there are two sets of memory pointers needed, one for each of the portions in the respective first and second memory sectors. The Lee '923 patent is silent on the use of such memory pointers and certainly does not describe a plurality of memory pointers for each portion of a sector. Lee certainly does not refer to a plurality of memory pointers associated with a portion of a sector of the array. The Examiner is not permitted to fashion a rejection merely by pointing to a position a place in the prior art which does not describe the claim structure and then say that such structures inherent in the function carried out. Clearly, such structures not inherent and the function can be implemented in many ways besides that which has been specifically claimed by Applicants.

Claim 12 adds the additional feature that one memory pointer is needed for each page into which the block is divided. Certainly the use of a single memory pointer per page is not known in the prior art nor has it been suggested or taught in any language in the Lee '923 patent. The use of a plurality of memory pages and each memory page having its own page pointer is a novel feature of the present invention which neither suggested by nor obvious from Lee the '923 patent or any other prior art.

Claim 13 is believed patentable in light of the Lee '923 patent. Claim 13 specifies a particular structure of having two FLASH memory portions which is subdivided each of which is divided into four memory blocks, each of which is subdivided into 64 memory pages and each of which is subdivided into 16 memory locations, each of which were able to store data bit. The

Lee '923 patent proposes not such subdivision and is silent on the subdivision in dividing of this memory. Accordingly, the rejection of claim 13 in light of the Lee patent is believed to be an error. Further, the Examiner's reference to the use of page pointers does not seem related to claim 13 since claim 13 does not deal with page pointers at all, but rather deals with the organization of the memory block.

Claim 16 is patentable for additional reasons beyond the patentability of the prior claims. Claim 16 specifies a particular organization of the memory structure which is novel and in addition, provides a novel method of writing into this memory structure. Claim 13 specifies an organization of the memory using a process which is completely foreign to the Lee '923 patent. In particular, the teaching of the present invention of claim 13 is an explanation of the emulation process in detail. The FLASH memory is divided into a first and second memory sector each of which contains a plurality of memory blocks and each memory block includes a plurality of memory pages and each of which includes a plurality of memory locations. While it is agreed that Lee does talk about pages and subpages, there is no teaching in Lee of the organization of the present invention of memory locations of the first level being organized into a plurality of memory locations representing the bit, the plurality of bites being organized into a page and then a plurality of pages being organized into a block and then a plurality of blocks being organized into a sector. Following this division of the FLASH memory cell, claim 16 specifies additional steps, which are taken none of which are obvious in nor taught in the Lee '923 patent. Specifically, claim 16 specifies that a page address is assigned to each of the first and second memory page sectors, but is shared by a corresponding page in each of the memory blocks, a feature in which the Lee '923 patent is completely silent. Further, claim 16 goes on to specify that a data page is written into the first memory block of the first memory sector in response to a first write instruction and then, in response to a second write instruction data is written to the selected page address of a second memory block within the same first memory sector. The Lee '923 patent does not describe such a sequence of method steps and claim 16 is believed patentable in light of the art.

Claim 17 is believed patentable for reasons beyond the patentability of claim 16. In particular, claim 17 provides the additional steps of the swap mechanism wherein the data is

swapped between the two FLASH sectors. There is nothing similar in Lee. Lee has no concept of the swapping of data and response to such a write instruction and no disclosure of concept of the emulation. One of the reasons is that the Lee '923 patent does not need to perform such emulation because he has altered his memory structure to provide direct erasing of the individual bits. The present invention does not have such a hardware structure rather, the present invention uses a normal FLASH memory array and carries out the three sequences of step as specified in claim 17 in order to do a swap between the memory blocks in a first sector and the memory blocks in a second sector.

Claim 18 is clearly patentable in light of the prior art. The Examiner takes the view that the use of the pointers is found in column 7, lines 42, to column 8, line 14. Applicants strongly disagree. As previously pointed out, the use of such pointers is not inherent and indeed, claim 18 specifies not pointers in general, but very specific steps for the use of pointers. In particular, claim 18 specifies a page pointer that reflects which memory page in a set has been most recently updated and then, in response to each write instruction determines which page pointers associated with the selected page address and further determines from the page pointer which memory page of the set of memory pages is next to be updated and writes the data into the correct memory page. No such discussion is present in the Lee '923 patent and the claims are clearly believed patentable in light thereof.

Claim 19 is believed patentable for reasons beyond the patentability of claim 16. The overall function of claim 19 is a method which hides from the user the erasing of the currently unused sector, while the EEPROM data is mapped to the other sector. The user is not able to see the emulation because the erasing of the second memory sector is occurring while updating the memory pages of the first memory sector. This transparent operation is completely foreign to the Lee '923 method of operation and cannot be accomplished by a structure. Clearly, claim 19 is patentable in light of the prior art.

Claim 20 is patentable for reasons as claim 19 and even for additional reasons beyond the patentability of claim 19. According to claim 20 there is a splitting of the erase operation into end phases, typically four phases however a different number of phases could be used. Each phase is hidden in a page update operation from the user point of view in order to not

increase the EEPROM write time. This is a completely new idea and a completely novel concept. There is nothing similar in Lee nor anything that can be compared to it in any prior art reference. Claim 20 is clearly patentable in light of the prior art.

Newly submitted claims 21-24 are also believed patentable in light of the art. Claim 22 specifies that a NOR FLASH array is the type of array which is used and that the state machine is used for the loading of hard-coded addresses in storage registers which are read and updated by the microcontroller during the reset phase. The microcontroller controls the data access to and from the addressing of the FLASH memory array whereas the state machine is coupled to an address controller and its coupled for outputting the control signals to the address counter. This particular organization of the microcontroller and the state machine are not discussed in the Lee '923 patent. Lee does not use nor disclose such a state machine nor the organization of the state machine with hard-coded addresses and storage registers which are read and updated by the microcontroller.

Claim 24 as submitted as specifying the NOR FLASH memory array being of the type that permits simultaneous erasing of all cells in an entire sector but does not permit simultaneous erasing of less than all cells in a sector. This particular structure is distinctly different from that of the Lee '923 patent. In particular, in the Lee '923 patent there is no concept of having an entire sector which cannot be simultaneously erased. Rather he changes his physical structure to permit individual erasing of individual cells, something the invention of claim 24 is not capable of doing. Claim 24 further specifies that at least two of the sectors are structured to emulate an EEPROM having by erasability. The emulation language of claim 24 is an important distinction of the Lee '923 patent. According to claim 24, an EEPROM is emulated, not constructed. In other words, a NOR FLASH memory array is made to emulate and look as if it is an EEPROM when in fact the array remains a NOR FLASH memory array in each respect. Claim 24 is therefore believed patentable in light of the Lee '923 patent.

The Examiner is not permitted to reject an entire claim just by saying it is inherent.

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Reply to Office Action dated June 18, 2003

It is believed that all claims now presented are patentable and allowance is respectfully requested.

Respectfully submitted,

Maurizio Peri et al.

SEED Intellectual Property Law Group PLLC

David V. Carlson
Registration No. 31,153

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Enclosure:
Postcard

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031

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